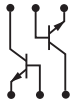
CMLT5088EM

SURFACE MOUNT
DUAL, MATCHED
NPN SILICON TRANSISTORS

PICOmini™



SOT-563 CASE

• Device is ***Halogen Free*** by design

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLT5088EM consists of two individual, isolated 5088E NPN silicon transistors with matched $V_{BE(ON)}$ characteristics. This device is designed for applications requiring high gain and low noise.

MARKING CODE: 88M

FEATURES:

• Transistor pair matched for $V_{BE(ON)}$

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	100	mA
Power Dissipation	P_D	350	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	357	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CBO}	V_{CB}=20V			50	nA
I_{EBO}	V_{EB}=3.0V			50	nA
BV_{CBO}	I_C=100μA	50	135		V
BV_{CEO}	I_C=1.0mA	50	65		V
BV_{EBO}	I_E=100μA	5.0	8.7		V
$V_{CE(SAT)}$	I_C=10mA, I_B=1.0mA		45	100	mV
$V_{CE(SAT)}$	I_C=100mA, I_B=10mA		110	400	mV
$V_{BE(SAT)}$	I_C=10mA, I_B=1.0mA		700	800	mV
h_{FE}	V_{CE}=5.0V, I_C=0.1mA	300	430	900	
h_{FE}	V_{CE}=5.0V, I_C=1.0mA	300	435		
h_{FE}	V_{CE}=5.0V, I_C=10mA	300	430		
h_{FE}	V_{CE}=5.0V, I_C=100mA	50	125		
f_T	V_{CE}=5.0V, I_C=500μA, f=20MHz	100			MHz
C_{ob}	V_{CB}=5.0V, I_E=0, f=1.0MHz			4.0	pF
C_{ib}	V_{BE}=0.5V, I_C=0, f=1.0MHz			15	pF
h_{fe}	V_{CE}=5.0V, I_C=1.0mA, f=1.0kHz	350		1400	
NF	V_{CE}=5.0V, I_C=100μA, R_S=10kΩ f=10Hz to 15.7kHz			3.0	dB

MATCHING CHARACTERISTICS:

SYMBOL	**TEST CONDITIONS**	**MIN**	**MAX**	**UNITS**
$\lvert V_{BE1}-V_{BE2}\rvert$	V_{CE}=5.0V, I_C=1.0μA		10	mV
$\lvert V_{BE1}-V_{BE2}\rvert$	V_{CE}=5.0V, I_C=5.0μA		10	mV
$\lvert V_{BE1}-V_{BE2}\rvert$	V_{CE}=5.0V, I_C=10μA		10	mV
$\lvert V_{BE1}-V_{BE2}\rvert$	V_{CE}=5.0V, I_C=100μA		10	mV

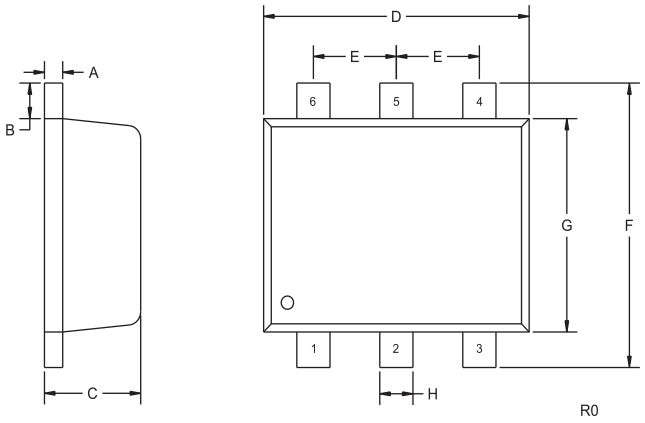
R0 (14-September 2009)

Central™
Semiconductor Corp.

CMLT5088EM

SURFACE MOUNT
DUAL, MATCHED
NPN SILICON TRANSISTORS

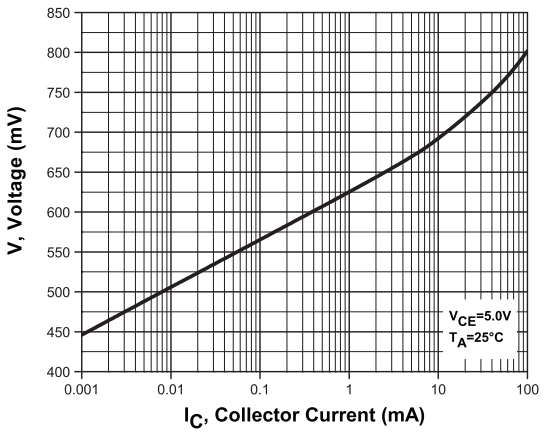
SOT-563 CASE - MECHANICAL OUTLINE



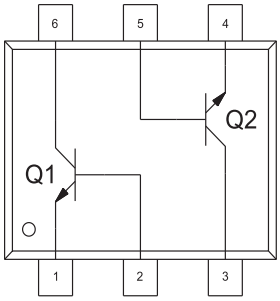
DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

CMLT5088EM Typical $V_{BE(ON)}$



PIN CONFIGURATION



LEAD CODE:
1) EMITTER Q1
2) BASE Q1
3) COLLECTOR Q2
4) EMITTER Q2
5) BASE Q2
6) COLLECTOR Q1

MARKING CODE: 88M

R0 (14-September 2009)